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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,939	07/31/2003	Gerard Chauvel	TI-35710 (1962-05423)	9644

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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,939	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,10-12,14 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,10-12,14 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-7, 10-12, 14, and 17-20 are pending.

2. The office acknowledges the following papers:

Specification, drawing, claims, and arguments filed 6/23/2006.

Withdrawn objections and rejections

3. The drawing objections have been withdrawn due to the amendment.

4. The specification objections have been withdrawn due to amendments and claim 8 being cancelled.

New Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3, 12, and 19 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "the local variables associated with the called method use data cache memory space marked as valid and previously used by local variables associated with completed methods, said data cache memory space marked as valid thereby avoiding generating a cache miss upon said local variables associated with the called method using said data cache memory space" is unclear. It's unclear if this limitation is to be interpreted as a method call will never result in generating a miss or if some method calls don't generate a miss. The

specification doesn't support method calls never generating a miss. If enough nested methods are called, then the D-RAMSET will fill up from storing all of the local variables from the method calls. This will result in some of the local variables being saved away in main memory, which will later generate a miss on local variables (Specifications paragraph 47). For claim interpretation, the limitation will be interpreted as some method calls don't generate a miss.

New Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 5-7, 10-12, 14, and 17-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Jain (U.S. 6,954,873).

9. As per claim 1:

Feierbach disclosed a system, comprising:

A first processor (Feierbach: Figure 2 element 204, column 6 lines 53-67 continued to column 7 lines 1-7);

A second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core (Feierbach: Figure 2 elements 104 and 210, column 6 lines 53-67 continued to column 7 lines 1-7);

Memory coupled to, and shared by, the first and second processors (Feierbach: Figure 2 element 212, column 6 lines 53-65)(The data cache is shared by the two processors.); and

A synchronization unit coupled to the first and second processors, said synchronization unit synchronizes the execution of the first and second processors (Feierbach: Figure 4 element 402, column 10 lines 25-55)(The copy unit monitors data accesses and ensures that data is properly exchanged between processors and other memory units. Thus having the same functionality.);

Wherein the second processor executes stack-based instructions (Feierbach: Figure 2 element 202, column 6 lines 53-65) while the first processor executes one or more tasks (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1, column 3 lines 20-67) wherein the first processor manages the memory via an operating system that executes only on the first processor (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1 elements 44a-b, column 3 lines 20-67)(Yung manages memory through the hardware memory management units. An operating system manages memory through software. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the processor of Yung could have managed memory from software using an operating system instead of hardware using the memory management units.) and the second processor executes a virtual machine that controls the execution of a program on the second processor (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S.

6,021,469))(Tremblay: Figure 1 element 100, column 5 lines 35-54)(The stack processor runs a virtual machine that controls the execution of instructions.).

Feierbach failed to teach the first processor executes a virtual machine that controls the execution of a program on the second processor and wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode.

However, Seal disclosed the first processor executes a virtual machine that controls the execution of a program on the second processor (Seal: Figure 18 element 326, column 16 lines 38-48; Figure 20, column 17 lines 38-67)(The processor includes a virtual machine to execute Java bytecodes. Some of the instructions can't be run on the processor, and are executed by software. Thus having the same functionality.).

An advantage of having the first processor process Java bytecodes through acceleration techniques is that the instructions will run faster on the hardware as opposed to the software executing the instructions (Seal: Column 1 lines 19-47). The instructions that are too complex to be executed on hardware are sent off to be executed on software (Seal: Column 1 lines 19-47). One of ordinary skill in the art would have been motivated to use a virtual machine to assist in accelerating Java bytecode instructions for the benefit of increased performance from the accelerated instructions being executed in hardware. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a virtual machine to help accelerate Java bytecodes for the advantage of increased performance.

Feierbach and Seal failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode.

However, Jain disclosed wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode (Jain: Figure 6a, column 3 lines 6-34)(By entering the wait stage, it's inherent that performance will be reduced because no instructions will be processed. In addition, Jain disclosed that the clocks are gated upon the wait signal, which causes the clock to stop upon detecting a wait signal, which will also inherently result in a power reduction from the clocks being gated.).

The advantage of using a synchronization unit to check data accesses is to avoid accessing corrupt or old data (Jain: Column 1 lines 49-58). The use of a wait signal can tell another processor that a current piece of data is being used elsewhere. One of ordinary skill in the art would have been motivated to check memory accesses and use wait signals for the advantage of upholding data integrity. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement wait signals for processors accessing data for the advantage of preventing data corruption and upholding data integrity.

10. As per claim 2:

Feierbach and Seal disclosed the system of claim 1 wherein the second

processor comprises an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11).

11. As per claim 3:

Feierbach and Seal disclosed the system of claim 2 wherein the second processor executes methods (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11) and wherein when a new method is called by the second processor, the local variables associated with the called method use data cache memory space marked as valid and previously used by local variables associated with completed methods, said data cache memory space marked as valid thereby avoiding generating a cache miss upon said local variables associated with the called method using said data cache memory space (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11)(The stack cache won't generate a miss as long as the stack cache isn't filled up with storage from other nested methods. It's obvious to one of ordinary skill in the art that the stack cache must include some sort of valid flag to indicate that memory is currently allocated to another method. If there was no valid flag, then enough nested calls could occur where the nested call would overwrite data from another method because it otherwise has no way of knowing if the data is being used elsewhere. This scenario results in the processor failing from losing data.).

12. As per claim 5:

Feierbach and Seal disclosed the system of claim 1 wherein the stack-based instructions comprise Java bytecodes (Feierbach: Column 5 lines 4-29) and the first processor comprises a RISC processor (Seal: Figure 10 element 12, column 5 lines 60-67 continued to column 6 lines 1-9) so that the RISC processor executes one or more tasks while the second processor executes Java code.

13. As per claim 6:

Feierbach and Seal disclosed the system of claim 1 further including a main stack residing outside the second processor's core and coupled to the stack storage in the second processor's core (Feierbach: Figure 2 element 212, column 7 lines 8-18).

14. As per claim 7:

Feierbach and Seal disclosed the system of claim 6 wherein the stack storage in the second processor's core provides an operand to execute a stack-based instruction in the second processor (Feierbach: Figure 2 element 210, column 7 lines 50-65).

15. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

16. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

17. As per claim 12:

Claim 12 essentially recites the same limitations of claim 3. Therefore, claim 12 is rejected for the same reasons as claim 3.

18. As per claim 14:

Claim 14 essentially recites the same limitations of claims 6-7. Therefore, claim 14 is rejected for the same reasons as claims 6-7.

19. As per claims 17-18:

Claim 17-18 essentially recites the same limitations of claim 1-2. Therefore, claim 17-18 is rejected for the same reasons as claim 1-2.

20. As per claim 19:

Claim 19 essentially recites the same limitations of claim 3. Therefore, claim 19 is rejected for the same reasons as claim 3.

21. As per claim 20:

Feierbach, Seal, and Jain disclosed the system of claim 1 wherein a clock internal to the first processor is disabled thereby effectuating the reduced power or reduced performance mode (Jain: Figure 6a, column 3 lines 6-34)(By entering the wait stage, it's inherent that performance will be reduced because no instructions will be processed. In addition, Jain disclosed that the clocks are gated upon the wait signal, which causes the clock to stop upon detecting a wait signal, which will also inherently result in a power reduction from the clocks being gated.).

Response to Arguments

22. The arguments presented by Applicant in the response, received on 6/23/2006 are not considered persuasive.

23. Applicant argues that "Feierbach fails to teach the stack residing in the processor core."

This argument is not found to be persuasive for the following reason. The processor core isn't defined as element 202. Element 202 simply contains execution elements to process instructions. Element 104 is the processor core and the stack is contained within it. Further proof of this is seen by elements 208 and 204. It's inherent that the register file is in the processor core because it's also contained within element 104.

24. Applicant argues that "Neither Yung nor Feierbach disclosed a processor executing an operating system."

This argument is not found to be persuasive for the following reason. Yung manages memory through the hardware memory management units. An operating system manages memory through software. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the processor of Yung could have managed memory from software using an operating system instead of hardware using the memory management units.

25. Applicant argues that "Jain fails to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode."

This argument is not found to be persuasive for the following reason. By entering the wait stage, it's inherent that performance will be reduced because no instructions will be processed. In addition, Jain disclosed that the clocks are gated upon the wait signal, which causes the clock to stop upon detecting a wait signal, which will also inherently result in a power reduction from the clocks being gated.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

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